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Abstract
Nowadays the digital video and image technology is becoming the essential part to human life. As the development and demand of the technology, the good quality of digital image is becoming more and more required. However, the high-compression video often loses part of the data during deciding process, and it causes blocking effects in images. The blocking effect makes the discontinuous phenomenon between the blocks in an image. Therefore, we need a deblocking filter to reduce the blocking effect and maintain the image quality.
This paper proposes a novel hardware construction for high performance consideration to enhance the efficiency of deblocking filter for H.264/AVC decoder. We use a new block-border processing order to save the cost and increase the efficiency. The experimental results show that our method has the improvement of 15% in performance as comparing to the Basic PBSR （Pipeline Buffer Shift Registers, PBSR） [20]. Also the hardware requirement of register array in our method can be saved about 30 %.
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